REMARKS

Claims 1 - 14 are pending in this application, of which claims 4-11 have been withdrawn from consideration. Reconsideration in view of the following remarks is respectfully requested. It is believed that this Request for Reconsideration is fully responsive to the Office Action dated **January 10, 2003**.

As to the Merits:

As to the merits of this case, while the Examiner has withdrawn his previous rejections based on Hong ('879), the Examiner now relies on the newly cited references of Hong, et al. (U.S. Patent No. 5,614,746) and Hu, et al (U.S. Patent No. 5,511,020) in setting forth the following rejections:

1. Claims 1, 3 and 12 - 14 stand rejected under 35 U.S.C. §103(a) as being obvious over by Hong ('746) in view of Hu, et al.; and

2. Claim 2 stands rejected under 35 U.S.C. §103(a) is being unpatentable over Hong ('746) and Hu in view of Shigyo (of record).

Each of these rejection is respectfully traversed.

It is respectfully submitted that the Examiner's reliance on Hong ('746) for teaching the features of claims 1, 12 and 14 concerning *a pair of impurity doped regions formed in a surface layer of said semiconductor substrate on both sides of a gate structure including said floating gate electrode and said first control gate electrode* is unfounded.

More specifically, in Hong ('746) the pair of impurity doped regions 36 are not formed on both sides of a gate structure including the first control gate electrode since the first control gate electrode 40 exists on top of the impurity regions 36. In fact, Hong ('746) does not disclose a gate structure including a floating gate electrode and a first control gate electrode, as called for in independent claims 1, 12 and 14.

This is in contrast to the present claimed invention in which, for example, as illustrated in Fig. 1, the first impurity doped regions 21 and 22 are formed on both sides of a gate structure including floating gate electrode 5 and first control gate electrode 11.

Further, while the Examiner properly acknowledges that "Hong et al. does not disclose the tunneling insulating film having a thickness thin enough to transmit carriers therethrough by a direct tunneling phenomenon,"[1] the Examiner relies on the secondary reference of Hu for teaching the above-noted drawbacks and deficiencies of Hong.

---

[1]Please see, the last two lines of page 2 of the outstanding Action.

That is, the Examiner takes the position that it would have been obvious to a person having ordinary skill in the art at the time of the invention was made to modify the memory device of Hong having a thin direct tunneling insulating film as taught by Hu. However, it is respectfully submitted that it would **not** have been obvious because of the following reason.

In claim 1, the gate insulating film covers a partial surface area of the semiconductor substrate on **both sides** of the floating gate electrode. The first control gate electrode is disposed on the gate insulating film over the partial surface area of the semiconductor substrate on **both sides** of the gate electrode. A pair of impurity doped regions are formed in the surface layer of the semiconductor substrate on both sides of the gate structure including the floating gate electrode and the first control gate electrode. Therefore, each of the impurity doped regions is located apart from the floating gate electrode because the first control gate electrode is allocated between the floating gate electrode and the impurity doped regions. The invention as defined in claims 12 and 14 also includes the same features as claim 1.

In Fig. 2 of Hong, the edge of the floating gate 24 is adjacent to one S/D region 36" (column 4, lines 43-44). In such structure, if the tunnel oxide layer 22 is replaced by the direct tunneling dielectric 102 of Hu, electrons accumulated in the floating gate electrode easily enter the S/D region 36" through the direct tunneling dielectric 102 by the direct tunneling phenomenon. Therefore, electrons in the floating gate electrode cannot be retained therein for a long time.

As describe above, if the tunnel oxide layer 22 is replaced by the direct tunneling dielectric 102 of Hu, Hong's device cannot work as a flash memory. Therefore, it would not have been obvious to modify the memory device of Hong having a thin direct tunneling insulating film as taught by Hu.

In addition, the Examiner insists that some claim features of claims 1 and 3 constitute functional language and are non-limiting since it has been held that claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. However, it is respectfully submitted that the phrases the Examiner points out do not limit function but limit the thickness of films.

Thus, for at least these reasons, it is respectfully asserted that the prior art fails to teach or suggest recitations of claims 1 - 3 and 12 - 14, and request that the Examiner allow these claims, along with the entire application, to issue. Accordingly, withdrawal of the rejection of claims 1 - 3 and 12 - 14 under 35 U.S.C. §103 and is respectfully solicited.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully Submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP

Thomas E. Brown
Attorney for Applicant
Reg. No. 44,450

TEB/kal
Atty. Docket No. **001497**
Suite 1000,1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930

23850
PATENT TRADEMARK OFFICE

H:\FLOATERS\TEB\teb\00\001497\MAR03Amendment